WHAT IS CLAIMED IS:

1. A semiconductor memory device with a built-in self test circuit, comprising:

a semiconductor substrate;

a memory cell array formed on said semiconductor substrate;

an input buffer provided on said semiconductor substrate to receive externally applied data;

a test circuit coupled to said memory cell array and said input buffer on said semiconductor substrate to store a program received via said input buffer and generating test data of said memory cell array according to the stored program to carry out testing of said memory cell array; and

a select circuit selectively applying to said memory cell array test data applied from said test circuit and data applied from said input buffer according to whether in a test operation or a normal operation.

2. The semiconductor memory device according to claim 1, wherein said test circuit comprises

a rewritable instruction memory provided on said semiconductor substrate to store said program,

a test pattern generation circuit provided coupled to said instruction memory on said semiconductor substrate to generate and apply to said select circuit test data and a command and address for testing to write into each memory cell of said memory cell array according to the program stored in said instruction memory, and

a controller connected to said input buffer and operating in response to an externally applied control signal via said input buffer so as to control writing of a program applied via said input buffer into said instruction memory and operation of said instruction memory and said test pattern generation circuit in a test;

said semiconductor memory device further comprises a readout circuit connected to said memory cell array and said test circuit, and responsive to control by said controller to read out and provide to a test

device outside said semiconductor memory device data from said memory cell.

3. The semiconductor memory device according to claim 2, wherein said test pattern generation circuit, said instruction memory, said memory cell array and said readout circuit operate in synchronization with a frequency-multiplied signal clock which is an operating clock signal of said controller multiplied by a predetermined factor.

4. The semiconductor memory device according to claim 3, wherein said test pattern generation circuit controls said readout circuit so that data from each of memory cells is repeatedly output for at least a number of times identical to said predetermined factor in synchronization with said frequency-multiplied clock signal and in response to an address of each of said memory cells scrambled to allow said test device to receive data at a predetermined order.

5. The semiconductor memory device according to claim 2, further comprising a plurality of control signal input terminals to receive a signal to control reading and writing of data with respect to said memory cell array and load data including the program stored in said test circuit from an external source, each said input terminal being connected to an input of said input buffer,

wherein the number of said control signal input terminals is smaller than the number of bits of each instruction stored in said test circuit,

said load data is applied to said plurality of control signal input terminals in a form where each instruction is divided into a number of bits not more than the number of said plurality of control signal input terminals, and

said controller responds to an externally applied load start control signal via said plurality of control signal input terminals and said input buffer so as to restore and store into said instruction memory each instruction of said program from the divided instruction applied via said

plurality of control signal input terminals and said input buffer.

6. The semiconductor memory device according to claim 2, wherein said load data includes input/output combination data to carry out testing of said memory cell array in addition to said program executed by said test circuit,

said readout circuit includes a plurality of input/output combination test circuits for writing test data corresponding to said input/output combination data into said memory cell array to determine whether the data read out from said memory cell array are correct or not, and

said controller causes said test circuit to store said program and applies said input/output combination data to said plurality of input/output combination test circuits.

7. The semiconductor memory device according to claim 6, wherein said test circuit can output expected value master data ; and

each of said plurality of input/output combination test circuits comprises

a register to store input/output combination data,

a write driver performing a logic operation between said expected value master data and the input/output combination data stored in said register, and

a determination circuit to determine whether the corresponding data read out from said memory cell array is correct or not by comparing the corresponding data with a value obtained by performing the logic operation between said expected value master data and the input/output combination data stored in said register.

8. The semiconductor memory device according to claim 5, wherein

said load data comprises mode data to set an operational mode of said semiconductor memory device, and

said controller causes said instruction memory to store said program, and sets the operational mode of said semiconductor memory device

according to said mode data applied via said input buffer.

9. The semiconductor memory device according to claim 2, wherein said test pattern generation circuit comprises an address scrambler applying address scramble on a logical address of said memory cell array.

10. The semiconductor memory device according to claim 2, wherein said test pattern generation circuit comprises a data scrambler to carry out a predetermined operation on an address of each memory cell to effect data scramble for generating data to be written into each memory cell to test said memory cell array.

11. The semiconductor memory device according to claim 1, wherein said test circuit comprises

a rewritable instruction memory provided on said semiconductor substrate to store said program, and

an algorithmic pattern generator under control of said program to generate data of a bit pattern to be written into each memory cell of said memory cell array according to an algorithm including a repeating operation,

wherein said algorithmic pattern generator includes

a general-purpose register used to store data during said repeating operation, and

a reload register retaining a value written at a predetermined timing during said repeating operation into said general-purpose register.

12. The semiconductor memory device according to claim 1, wherein said test circuit comprises an operation control circuit receiving an external signal to control a repeating operation by said test circuit in a test with respect to said memory cell array in response to a value of said external signal.

13. The semiconductor memory device according to claim 1,

wherein an instruction set for said test circuit includes a conditional jump instruction,

said test circuit carrying out a delayed jump executing a branch operation by said conditional jump instruction at a cycle after the cycle where said conditional jump instruction has been executed.

14. The semiconductor memory device according to claim 1, wherein said test circuit comprises

a controller provided on said semiconductor substrate, and operating by a clock signal of a predetermined frequency,

a rewritable instruction memory provided on said semiconductor substrate to store said program, and operating by a frequency-multiplied clock signal which is a clock signal having said predetermined frequency multiplied by a predetermined factor, and

an algorithmic pattern generator provided on said semiconductor substrate and operating by said frequency-multiplied clock signal to generate test data and a control signal of said memory cell array according to a program stored in said instruction memory.

15. The semiconductor memory device according to claim 14, further comprising an input/output buffer providing test data generated by said pattern generator outside said semiconductor memory device.

16. The semiconductor memory device according to claim 1, wherein said test circuit indicates test pass at a first level of a test result signal and test fail at a second level of said test result signal,

wherein said test circuit drives said test result signal to said second level prior to output of a test result.

17. A method of executing testing of a memory cell array in a semiconductor memory device with a built-in self test circuit, said method comprising the steps of:

initiating reception of load data including a program defining a

procedure of test from outside said semiconductor memory device via predetermined number of pins in response to an externally applied first control signal,

sequentially receiving said load data and sequentially storing said load data into an instruction memory,

terminating reception and storage of load data in response to encountering information indicating termination of load data in said load data, and

executing a program included in said instruction memory in response to an externally applied second control signal to generate test pattern data of said memory cell array according to an algorithm realized by said program to carry out testing of said memory cell array.

18. The method according to claim 17, wherein the number of bits per one word of an instruction stored in said instruction memory is greater than the number of said pins,

wherein said step of storing includes the step of restoring an instruction included in said load data by sequentially storing the sequentially received load data into said instruction memory.

19. A method of providing data read out from a memory cell array in synchronization with a first clock signal of a first frequency to an external circuit that operates in synchronization with a second clock signal of a second frequency lower than said first frequency, wherein the ratio of said first frequency to said second frequency is a predetermined positive integer,

said method comprising the step of:

repeating for a plurality, identical to said predetermined positive integer, of times sequential output of a plurality, identical to said predetermined positive integer, of data items read out from said memory cell array one by one per one cycle of said first clock signal, said plurality of data items constituting a data block repeatedly read out one by one per one cycle of said second clock signal for said plurailty of times.

20. The method according to claim 19, further comprising the step of scrambling a read out address of data from said memory cell array by a predetermined manner.